

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-252744

(43)Date of publication of application : 09.09.1994

(51)Int.Cl.

H03K 19/21

G06F 7/04

G06G 7/60

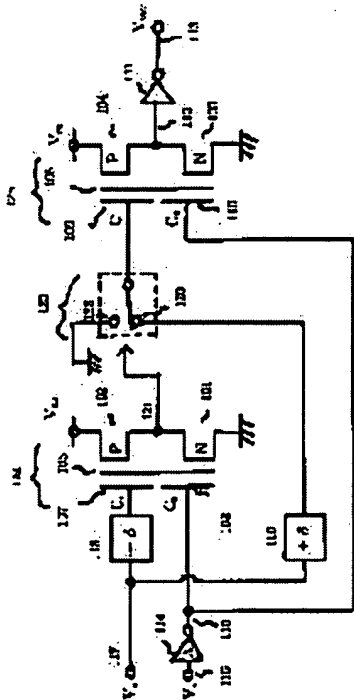
(21)Application number : 05-057748

(71)Applicant : SHIBATA SUNAO
OMI TADAHIRO

(22)Date of filing : 22.02.1993

(72)Inventor : SHIBATA SUNAO
KOTANI KOJI
OMI TADAHIRO

(54) SEMICONDUCTOR INTEGRATED CIRCUIT



(57)Abstract:

PURPOSE: To provide a semiconductor integrated circuit in which data matching is implemented at a high speed through the use of a simple circuit.

CONSTITUTION: The semiconductor integrated circuit having at least one 1st input terminal 117 and at least one 2nd input terminal 115 receiving a voltage signal, and at least one output terminal 113 to provide a predetermined signal at the output terminal 113 when a difference of numerals expressed by two sets of signals inputted respectively to the 1st and 2nd input terminals 117, 115 is smaller than a predetermined value includes at least two inverters 124, 125 comprising neuron MOS transistors (TRs) 101, 103 and is characterized in that the two sets of signals or signals subject to predetermined processing partly are inputted to at least one of input gates of each inverter.

LEGAL STATUS

[Date of request for examination]

21.02.2000

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than

the examiner's decision of rejection or
application converted registration]

[Date of final disposal for application]

[Patent number] 3278080

[Date of registration] 15.02.2002

[Number of appeal against examiner's decision
of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office